Atty. Docket No. MP0299
Application No: 10/634,218

Amendments to the Claims

Please amend Claims 1, 16, 24, 25, 30, 51, 57, and 88 as follows:

1. (Currently Amended) An architecture for transferring data from a first device to a second device, comprising:
   a) a clock recovery loop receiving said data from said first device, said clock recovery loop providing a recovered clock signal;
   b) a filter circuit configured to filter information from said recovered clock signal and provide a transmitter clock adjustment signal that adjusts [[said]]a transmitter clock signal in response to inputs from (i) said clock recovery loop and (ii) a transmitter clock circuit; and
   c) a transmitter in communication with said filter circuit, configured to receive said transmitter clock adjustment signal and transmit said data to said second device in accordance with said transmitter clock signal.

2. (Original) The architecture of claim 1, further comprising a receiver in communication with said clock recovery loop and said filter circuit, configured to receive said data from a network.

3. (Original) The architecture of claim 1, wherein said clock recovery loop comprises a first phase detector configured to determine a phase difference between said recovered clock signal and either a reference clock signal or said data.

4. (Original) The architecture of claim 3, wherein said clock recovery loop further comprises a recovered clock adjustment circuit configured to adjust said recovered clock signal in response to said phase difference.

5. (Original) The architecture of claim 4, wherein said recovered clock adjustment circuit provides a recovered clock adjustment signal in response to said phase difference.

6. (Original) The architecture of claim 5, wherein said input from said clock recovery loop comprises said recovered clock adjustment signal, and said filter circuit is further configured to filter said recovered clock adjustment signal.

7. (Original) The architecture of claim 6, wherein said filter circuit is further configured to provide said transmitter clock adjustment signal in response to said filtered recovered clock adjustment signal and said input from said transmitter clock circuit.

8. (Original) The architecture of claim 7, wherein said input from said transmitter clock circuit comprises said transmitter clock signal.

9. (Original) The architecture of claim 8, wherein said filter circuit provides said transmitter clock adjustment signal in further response to said recovered clock signal, said filter circuit being further configured to determine a phase difference between said transmitter clock signal and said recovered clock signal.

10. (Original) The architecture of claim 1, wherein said filter circuit comprises a jitter reduction circuit configured to reduce jitter in said input from said clock recovery loop and provide a filtered clock information signal in response thereto.

11. (Original) The architecture of claim 10, wherein said filter circuit further comprises a clock alignment block configured to (i) receive said recovered clock signal and said transmitter clock signal and (ii) provide a data transfer control signal in response thereto.

12. (Original) The architecture of claim 11, wherein said filter circuit further comprises a logic circuit configured to mathematically combine said data transfer control signal and

said filtered clock information signal and provide said transmitter clock adjustment signal in response thereto.

13. (Original) The architecture of claim 1, wherein said transmitter is configured to transmit serial data.

14. (Previously Presented) A circuit for facilitating data transfer, comprising:
   a) a clock alignment block configured to (i) receive first and second periodic signals comprising a recovered clock signal and a transmitter clock signal and (ii) provide a data transfer control signal in response thereto;
   b) a first filter circuit configured to receive first periodic signal information and provide a filtered clock information signal in response thereto; and
   c) a logic circuit configured to combine said data transfer control signal and said filtered clock information signal and provide an adjustment signal for said second periodic signal in response thereto.

15. (Canceled)

16. (Currently Amended) The circuit of Claim 14, wherein said clock alignment block comprises a ~~first~~-phase detector configured to receive said first and second periodic signals.

17. (Original) The circuit of Claim 16, wherein said clock alignment block further comprises a second filter circuit configured to filter an output of said phase detector and provide said data transfer control signal.

18. (Original) The circuit of Claim 17, wherein said second filter circuit comprises a multiplier configured to multiply said output of said phase detector by a first coefficient.

19. (Original) The circuit of Claim 18, wherein said second filter circuit further comprises a first integrator configured to integrate an output of said multiplier and provide said data transfer control signal.

20. (Original) The circuit of Claim 14, wherein said first filter circuit comprises a frequency tracking loop.

21. (Original) The circuit of Claim 20, wherein said frequency tracking loop comprises a first adder configured to add said first periodic signal information and said filtered clock information signal.

22. (Original) The circuit of Claim 21, wherein said frequency tracking loop further comprises a second multiplier configured to multiply an output of said first adder by a second coefficient.

23. (Original) The circuit of Claim 22, wherein said frequency tracking loop further comprises a second integrator configured to provide said filtered clock information signal.

24. (Currently Amended) The circuit of ~~Claim 21~~Claim 22, wherein said first filter circuit further comprises a phase adjustment circuit configured to receive said output of said first adder and provide a phase adjustment signal in response thereto.

25. (Currently Amended) The circuit of Claim 24, wherein said phase adjustment circuit comprises (i) a third multiplier configured to multiply [[an]]said output of said first adder by a third coefficient, and (ii) a third integrator configured to provide said phase adjustment signal.

26. (Previously Presented) The circuit of Claim 14, wherein said logic circuit comprises an adder.

27. (Original) A system, comprising:
a) the architecture of Claim 1; and
b) a receiver communicatively coupled to said clock recovery loop, configured to receive said data from a network and transfer said data to said transmitter.

28. (Previously Presented) The system of Claim 27, further comprising an oscillator configured to provide a reference clock signal to said transmitter and said clock recovery loop.

29. (Original) The system of Claim 27, embodied on a single integrated circuit.

30. (Currently Amended) The system of Claim 27, wherein said receiver is further configured to convert serial data from [[a]]said network to parallel data for the transmitter.

31. (Original) The system of Claim 30, wherein said receiver further comprises a deserializer operating in accordance with the recovered clock signal.

32. (Original) The system of Claim 30, wherein said transmitter is further configured to convert parallel data from the receiver to serial data for transmission to a destination device.

33. (Original) The system of Claim 32, wherein said transmitter further comprises a serializer operating in accordance with the transmitter clock signal.

34. (Original) The system of Claim 27, further comprising a first port communicatively coupled to said receiver and a second port communicatively coupled to said transmitter, each of said first and second ports being configured to communicate with one or more external devices.

35-41. (Canceled)

42. (Original) A network, comprising:
   a) a plurality of the systems of claim 27; and
   b) a plurality of storage or communications devices, each of said storage or communications devices being communicatively coupled to at least one of said systems.

43. (Original) The network of Claim 42, wherein said plurality of said systems are embodied on a single integrated circuit.

44. (Original) The network of Claim 42, wherein said plurality of said systems receives serial data from said plurality of storage or communications devices.

45. (Original) The network of claim 42, wherein a first one of said plurality of storage or communications devices operates at a first frequency, a second one of said plurality of storage or communications devices operates at a second frequency the same as or different from the first frequency, and said plurality of said systems operates at a third frequency the same as or different from either or both of the first and/or second frequencies.

46. (Original) The network of Claim 45, wherein each of said first and second devices and each of said plurality of said systems transmits serial data at a rate of at least 1 Gb/second.

47. (Original) The network of Claim 45, wherein each of said plurality of said systems transmits serial data at a rate F_3 that is about the same as at least one of a rate F_1 at which said first device transmits serial data and a rate F_2 at which said second device transmits serial data.

48. (Original) The network of Claim 42, further comprising a network controller or logic configured to select a first device of said plurality of storage or communications devices from which serial data is to be transmitted.

49. (Original) The network of Claim 48, wherein said network controller or logic is further configured to select a second device of said plurality of storage or communications devices to which serial data is to be transmitted.

50. (Original) The network of Claim 49, wherein said network controller or logic is further configured to select a data path through said plurality of said systems to receive said serial data from said first device and transmit said serial data to said second device.

51. (Currently Amended) An architecture for transferring data, comprising:

a) means for recovering a clock signal from said data;

b) means for filtering recovered clock signal information;

c) means for adjusting a transmitter clock in response to (i) ~~said~~ filtered recovered clock signal information, (ii) ~~said~~ a recovered clock signal and (iii) a transmitter clock signal; and

d) means for transmitting said data to an external device in accordance with said transmitter clock signal.

52. (Original) The architecture of claim 51, further comprising a means for receiving said data.

53. (Original) The architecture of claim 51, wherein said means for recovering comprises a means for determining a phase difference between said recovered clock signal and either a reference clock signal or said data.

54. (Original) The architecture of claim 53, wherein said means for recovering further comprises a means for adjusting said recovered clock signal in response to said phase difference.

55. (Original) The architecture of claim 54, wherein said means for filtering filters an output of said means for adjusting said recovered clock signal.

56. (Original) The architecture of claim 51, wherein said means for filtering is configured to reduce jitter in said recovered clock signal information.

57. (Currently Amended) The architecture of claim 51, wherein said means for adjusting a transmitter clock further comprises a means for determining [[said]]a difference between said recovered clock signal and said transmitter clock signal.

58. (Original) The architecture of claim 51, wherein said data comprises serial data.

59-70. (Canceled)

71. (Original) A system, comprising:
    a) the architecture of claim 51; and
    b) a means for receiving said data, communicatively coupled to said means for recovering said clock signal, configured to receive said data from a network and transfer said data to said means for transmitting.

72. (Previously Presented) The system of Claim 71, further comprising a means for providing a reference clock signal to said means for transmitting and said means for recovering said clock signal.

73. (Original) The system of Claim 71, wherein said means for receiving further comprises means for converting serial data to parallel data.

74. (Original) The system of Claim 73, wherein said means for transmitting further comprises means for converting parallel data from the means for receiving to serial data.

75. (Original) The system of Claim 71, further comprising (i) first means for communicating with one or more first external devices, communicatively coupled to said means for receiving and (ii) second port means for communicating with one or more second external devices, communicatively coupled to said means for transmitting.

76-81. (Canceled)

82. (Original) A network, comprising:
    a) a plurality of the systems of Claim 71; and
    b) a plurality of means for data storing or data communications, each of said means for data storing or data communications being communicatively coupled to at least one of said systems.

83. (Original) The network of Claim 82, wherein said each of said plurality of said systems receives serial data from said plurality of means for data storing or data communications.

84. (Original) The network of Claim 82, wherein a first one of said plurality of means for data storing or data communications operates at a first frequency, a second one of said plurality of means for data storing or data communications operates at a second frequency the same as or different from the first frequency, and said plurality of said systems operates at a third frequency the same as or different from either or both of the first and/or second frequencies.

85. (Original) The network of Claim 84, wherein each of said first and second means for data storing or data communications and each of said plurality of said systems transmits serial data at a rate of at least 1 Gb/second.

86. (Original) The network of Claim 84, wherein each of said plurality of said systems transmits serial data at a rate F_3 that is about the same as at least one of a rate F_1 at which said first means for data storing or data communications transmits serial data and a rate F_2 at which said second means for data storing or data communications transmits serial data.

87. (Original) The network of Claim 82, further comprising a means for controlling a network.

88. (Currently Amended) The network of Claim 87, wherein said means for controlling said network comprises means for selecting a first one of said plurality of means for data storing or data communications from which serial data is to be transmitted, a second one of said plurality of means for data storing or data communications to which serial data is

to be transmitted, and one of said systems to receive said serial data from said first means for data storing or data communications and transmit said serial data to said second means for data storing or data communications.

89-98. (Canceled)